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# Security Enhancement in Systems using 7T Static Random-Access Memory Cell

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**ABSTRACT:** A significant danger to computer security has emerged via the use of power analysis (PA) attacks, which enable covert data extraction by examining the current being used by the power source of the system. Many of these systems rely on embedded memories, often implemented using six-transistor (6T) static random-access memory (SRAM) cells. Conventional SRAM cells are vulnerable to side-channel attacks because the connection among their electrical characterization and written data allows them to be mapped. By integrating an extra transistor into the 6T SRAM cell, as well as two-phase write operations, we believe we may increase the SRAM's resilience and offer enhanced security in the face of these kinds of assaults. An in-house-developed 7T SRAM cell (which uses a 28 nm manufacturing process) outperforms traditional 6T SRAM in terms of reduced write energy standard deviation, achieving nearly 1000X lower variance in write "1" and "0" operations. The cell is capable of decreasing write energy by 39%–53%, and it also has a decrease in write latency of 19%–38% compared to existing power analysis resistance SRAM cells.

**KEYWORDS:** System on chip, Transistors, power analysis, static random access memory.

## I. INTRODUCTION

Modern systems-on-chips (SoCs) are designed to tackle the problems of many environments and applications. Starting with a complicated and rather well-protected automobile system, we move on to mobile devices with less resources and finally to a standalone network node. The transmission, processing, and storage of sensitive data is an area where each of these sectors has unique security needs. Consequently, researchers and businesses alike are increasingly worried about the safety of these electronic systems.

Because they take use of private knowledge about the physical behaviour of cryptographic devices, Side Channel Analysis (SCA) attacks pose a significant danger to these devices [1-2]. Because they only necessitate basic hardware and software, Power Analysis (PA) and Electromagnetic Analysis (EMA) assaults are strong forms of SCA [3–11]. The link between a device's internally processed and stored data and an immediate physical measurable quantity (such as radiation or current) can be used in PA and EMA attacks to extract secret or sensitive information.

Important for security, Secured Static Random-Access Memories (SRAM) can be created as a Root-Of-Trust component for storing or boot-loading a used for long-term secrets storage (on-chip SRAM macros), intermediate calculations (L0, L1 cache, Register files, FIFOs, etc.), or several other purposes. Additionally, security primitives including P/T-RNGs, SRAM-PUFs, and seed storage and loading are built using these. The authors in [12] shown that even in a secure-design, the system's security is compromised by instantiating insecure memory instances, which is a danger associated with employing an insecure memory. They proved that a real-world data-masked system is less secure when using a microprocessor's local register files, shift-registers, and tiny caches (L0 and L1). When sensitive data is exposed to higher-caches, as happens, for example, during a software implementation's load/store operation, this problem becomes more apparent and becomes a bigger difficulty.

It is often more advantageous to implement side-channel protection on low-level cache hierarchies when logic-layer protection is required. Many very large-scale integration (VLSI) system-on-chips (SoCs) [13] rely on low-level caches (e.g., embedded memories) to store data and instructions, and these caches are essential to many cryptographic systems (e.g., smart cards [14] and wireless networks using cryptography algorithms [15]). Consequently, there is paramount relevance in studying and designing protected embedded memory. The 6-transistor (6T) SRAM macrocell is the



standard for embedded memory in most systems. Due to the link between the data stored in the memory and the current pulled from the memory supply, traditional 6T SRAM cells are vulnerable to power/electromagnetic analysis assaults [16–17].

This makes them leak important information. Due to the extra devices used to reduce the correlation between the proceed data and the gate's power consumption, designing SCA-resilient digital circuits often results in significant area and power penalties [18]. However, these overheads are unmanageable when it comes to the design of secured embedded memories, which already cause area and power bottlenecks in many SoCs [19–20]. The majority of the literature on secured SRAM implementations has been on bitcell-level solutions, with suggestions for modifying SRAM cells to lessen data leakage from bitcell array supplies. The initial 6T SRAM implementation necessitated the insertion of extra devices, which led to substantial space and power overheads in these implementations. It is crucial to avoid architecturally encrypting or disguising memory content since it imposes substantial overhead and expenses. Lastly, foundries often employ "pushed" design criteria to further shrink the 6T SRAM cell; however, these rules are inapplicable when creating changed bitcells, leading to an even bigger area overhead when attempting to alter a design at the bit-cell level.

## II. METHODOLOGY

Recently, a new technique was used that employs cryptographic applications in devices where more sensitive information is stored and retrieved. Thus, in contrast to other power analysis methods, the connection of instantaneous current consumption power distribution devices and information leakages is clearly shown in its effect on the power analysis methods of calculating side channel signals. This paper describes a new security-oriented 7T SRAM cell design that includes two-phased write processes and minimizes correlation between written and stored data, and therefore conserves power. In the current 6T SRAM implementation, there is one power gate transistor for each memory cell. The proposed 7T cell will use an extra transistor to increase the total number of transistors, with single energy gate transistors per memory cell. This proposed work would develop a 7T Ram bit cell in 22nm CMOS technology with inline and 8-bit level operations in TANNER EDA Software. It will do so compared to the 6T SRAM bit cell it is replacing, which is also done in 22nm CMOS technology having single bit and 8-bit level operations.

### 2.1 7T SRAM Design

The circuit design and the operating waveform of a proposed cell system are shown in figures 1 and 2. The most notable aspect of the method is that an extra nMOS transistor has been added between the output of driver nMOS transistor of a memory cell and the source of the memory cell's nMOS transistors, which allows modest swings of bit lines during a write operation. This nMOS, which is in addition to the remainder of this document, is referred to as  $V_{ss}$ . When applied with a nMOS load transistor, a bit line is precharged to  $V_{DD} - V_{TN}$ . Afterwards, in a write operation where  $V_{tn}$  and  $DBL$  are the threshold voltage of a load nMOS and writing swing, respectively, the bit line is pushed down to  $V_{DD} - V_{TN} - DBL$ . Because the cells' access transistors cannot turn on during the write process, the duty cycle level should not be set to  $V_{DD}$ . Because there is no disparity between the operating voltage of bit lines in read phases which in write cycles, there is no extra power consumption if the read and write cycles alternate. SLC and WL are synced before the switch  $V_{ss}$  is switched off; this causes  $V_{ss}$  to be shut off before WL is at the highest point during a write cycle. The driver nMOS transistors will not draw current when the word line is active due of the switch.

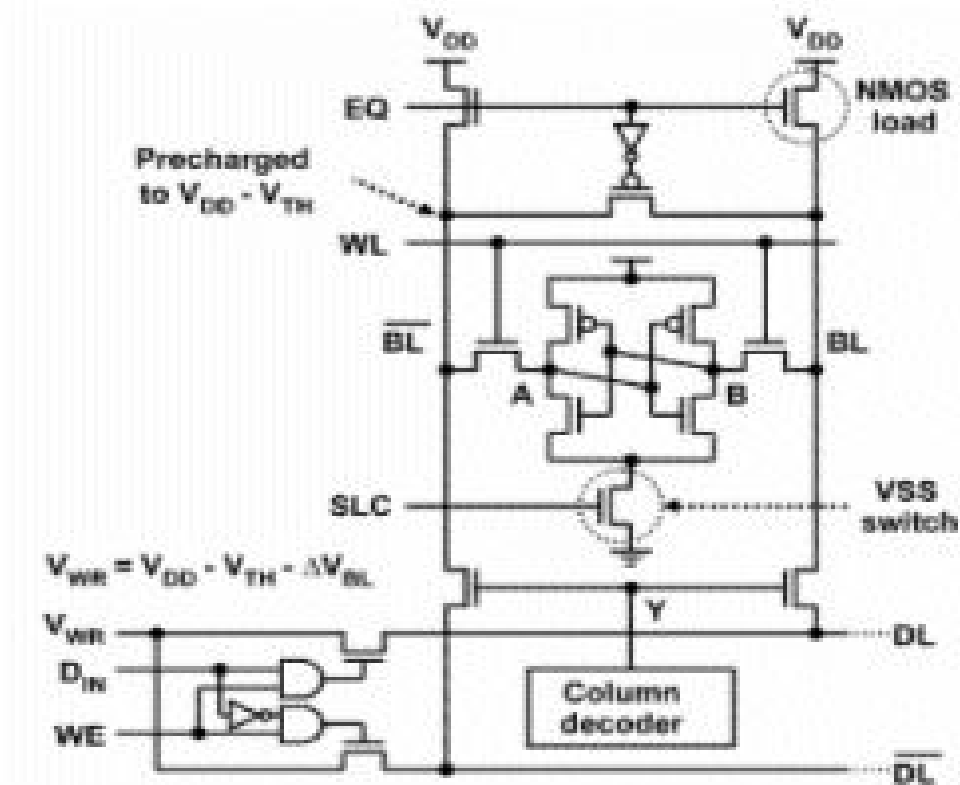


Figure 1. Overall Architecture of 7T SRAM cell

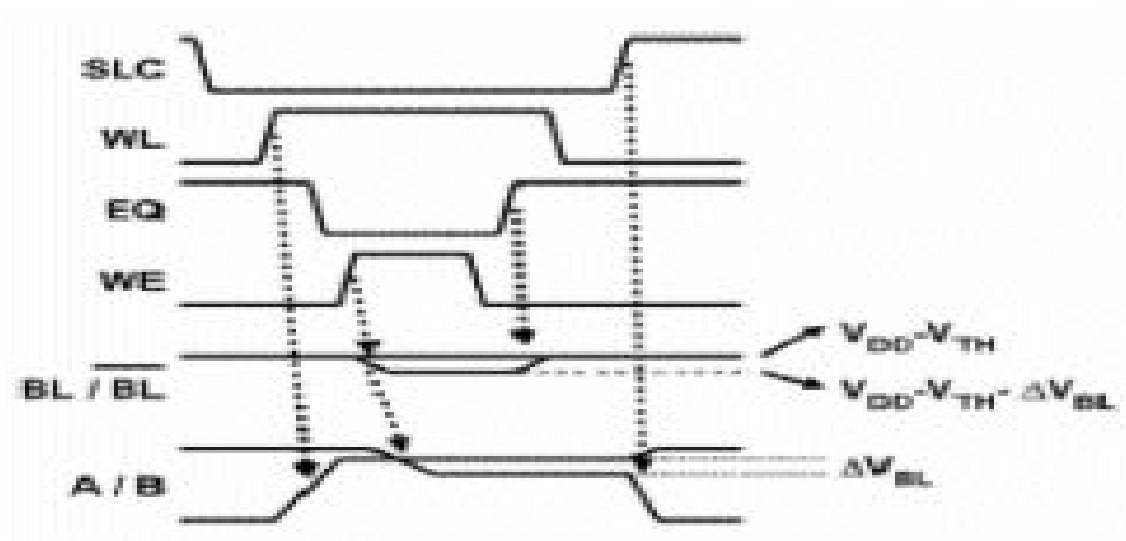


Figure 2. Write Cycle waveform

Once WL reaches a low point, SLC climbs back to high, and the swing on small-swing data is exaggerated until it fills the gap within a cell. To enable the cells to communicate with the active word-line, the cells that are linked to the word-line should be in a write cycle. For example, data stored in 192 cells becomes unstable while 64 cells are written if the numbers of cells linked to a word-line and to an SLC signal line are 64 and 256, respectively. In Fig. 3, you can see a dc-dc converter working with a voltage reference generator to bring the voltage level of  $V_{dd} - V_{tn} - DBL$  to the level indicated.

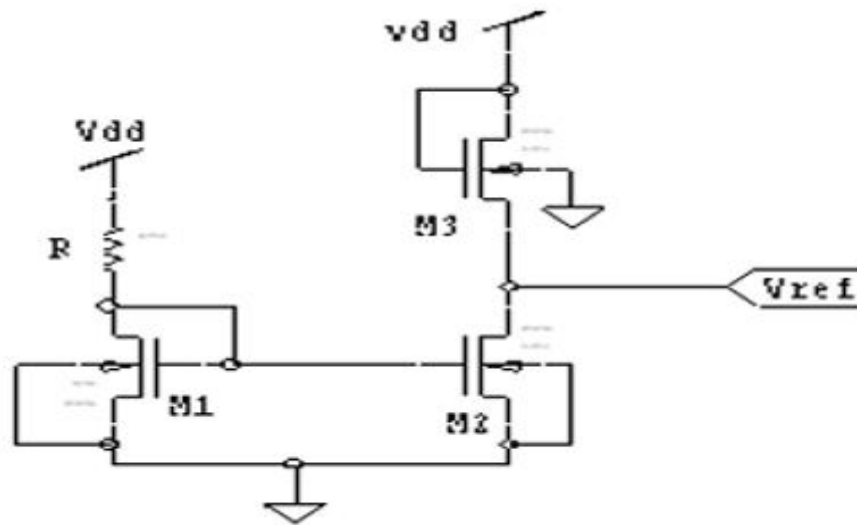


Figure 3. Write Voltage Generation Design

Each bit line receives voltage from the  $V_{wr}$  converter through the write circuit. The static power consumption of the voltage generator is quite high, but one generator is sufficient for the whole SRAM chip and the power overhead is insignificant.

By setting the source terminal of the cell driver nMOS transistor floating in write cycles, both the proposed 7T and the driving source line (DSL) cell [3] accomplish small-swing write operation. In contrast to the DSL system, the primary benefit of the suggested design is that it does not need half-prec-harging of bit lines, and it produces positive voltage. As a way to boost the current going to the nMOS transistor, a negative voltage is applied to the source node of the cell driver nMOS transistor during a read cycle. In devices with increased feature size, this causes the gate oxide of the nMOS transistor to be overstressed, resulting in decreased reliability. Pre-charging the bitlines may be avoided since it is utilized in the HS architecture. That is also beneficial because when the connected in series voltage level drops, the write error rate rises. This latter method is referred to as the "Switched Virtual GND Level" or SVGL (short for "Switched Virtual GND Level" or SVGL). Our approach is very different from the SVGL one in that way. To raise the transistors' operating voltage during write cycles, a source terminal of cell driver nMOS transistors is linked to a virtual-GND line, and its voltage is increased from ground level. A virtual-GND line works in tandem with a bitline in the SVGL scheme, while an SLC signal line travels alongside a wordline in the SAC approach. Since the virtual GND line is often longer than just a local wordline, the overhead in terms of delay, power, and area of driving the virtual GND line is considerable compared to the cost, power, and area of driving the SLC signal line. Another factor is that when the bit width is set to 8-bits, the number of active virtual ground lines is equal to the number of active SLC signal lines, while the frequency of activated virtual ground lines is equivalent to the number of activated virtual ground lines. Thus, the SAC (system in a May) system can have reduced voltage and faster speed than the SVGL (system in a Can) system.

## 2.2 Cell Design Consideration

In the proposed method, read latency, noise margin, and cell area are the most important considerations in cell design. It is mentioned beforehand that there are trade-offs between three design limits of the switch  $V_{ss}$  to  $b$  and  $N$ . This circuit

is from Figure 4 which illustrates the intended cell in a read cycle. There are seven nMOS transistors located along the read current route. These three transistors constitute a cell access transistors, a cell driver fets, and the switch's Vss. The first important design parameter  $b$  is found by defining  $b$  as the ratio of  $W_{sw}$  to  $W_d$ . Because the definition of  $B$  in this instance is technological-specific, any future debates about the field of technology may apply to any node in the technology tree. When  $W_d$  is set to  $3W_a$  in a typical six-transistor cell,  $b$  is practically limitless. Read current or static noise margins will be reduced by the installation of the switch having a finite value. Thus, it's obvious that greater read latency and noise margin result from bigger size, but the maximum value is limited by size restrictions. The second critical parameter  $N$ , pertains to a switch layout problem. Since overhead area takes up more than 20 percent of the space, you cannot put the switch cell by cell. The more cells in the same neighborhood, the more a common resource should be spread.

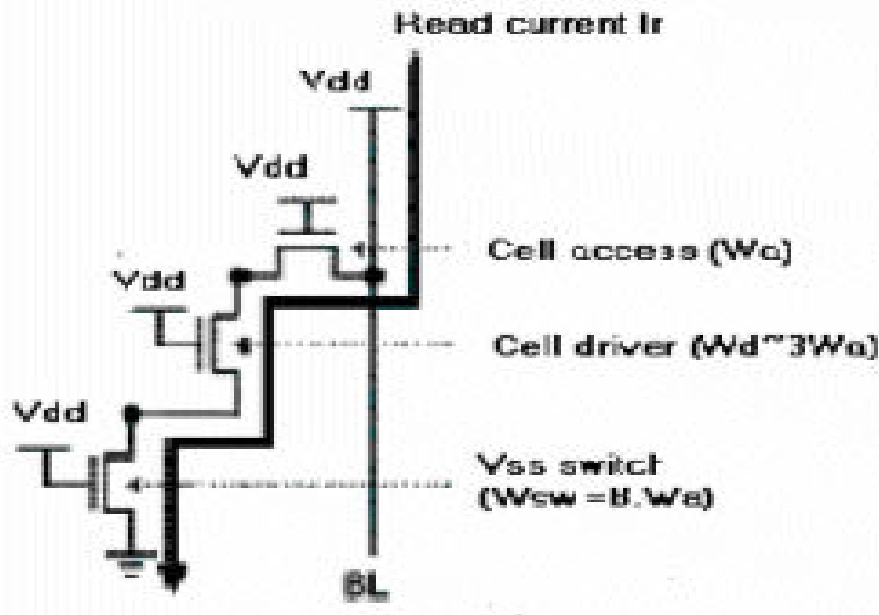


Figure 4. Read Current path of a seven-transistor cell

The three components in each row are responsible for the area penalty. The SLC signal line, the switches itself, and the common - base line which links each cell to the switch are all together referred to as the SLC signal line. This is the most straightforward method to do it, just make the value's maximum equal to the bit width. But in reality, it is difficult to configure in this way because of the following reasons. In figure 4, we see the shared switch structure's read current path. The total current that travels via the common - base line is equal to  $N$  while the device is reading.

### III. RESULTS AND DISCUSSION

As a result of the 6T SRAM cell's information leakage, we propose a modified 7T SRAM cell that incorporates a two-phase write operation, which includes an equalization phase and a write phase, and causes a significant reduction in the amount of current wasted during the write operation, compared to using the 6T SRAM cell directly.

#### 7T SRAM

The suggested 7T SRAM cell is shown in Fig. 5. To prevent power dissipation during the write process, a power gate PMOS transistor (PG) is utilized to turn off the whole memory word ( $V_{DD}$ ) voltage supply. The original 6T SRAM system includes a transistor PPC connected to the base of Q and QB that short-circuits Q and QB during the equalization phase. The PC voltage signal is used to turn off PG, thereby removing unnecessary power usage from the power supply, and then to turn on PPC to do voltage equalization between Q and QB. When the write process occurs in

its second phase, PC is discharged to charge  $V_{DD}$ , turn off PPC, and then is charged to transfer data from BL and BLB to Q and QB.

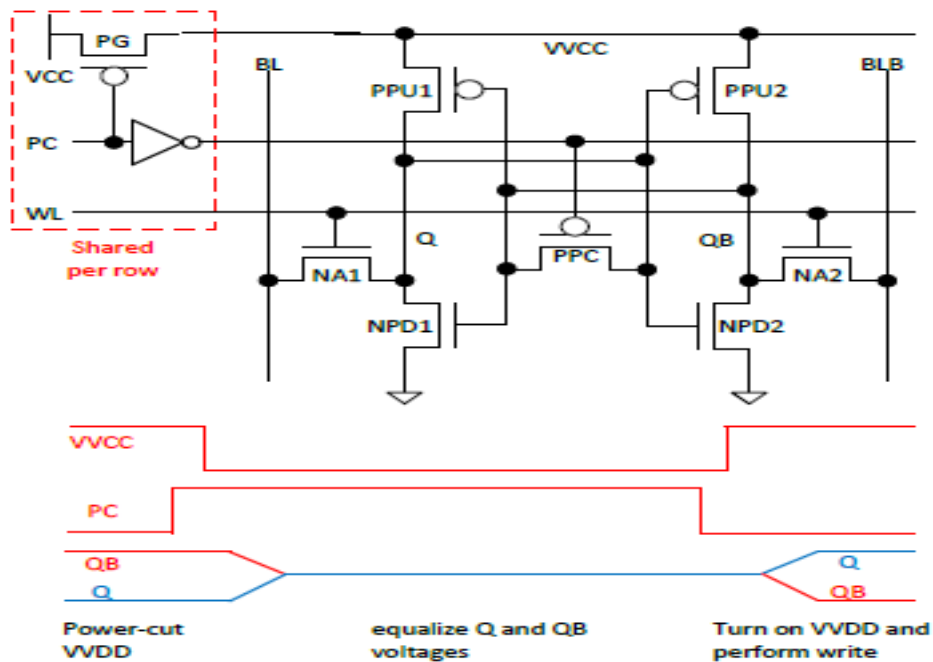


Figure 5. Basic operation of 7T SRAM Cell

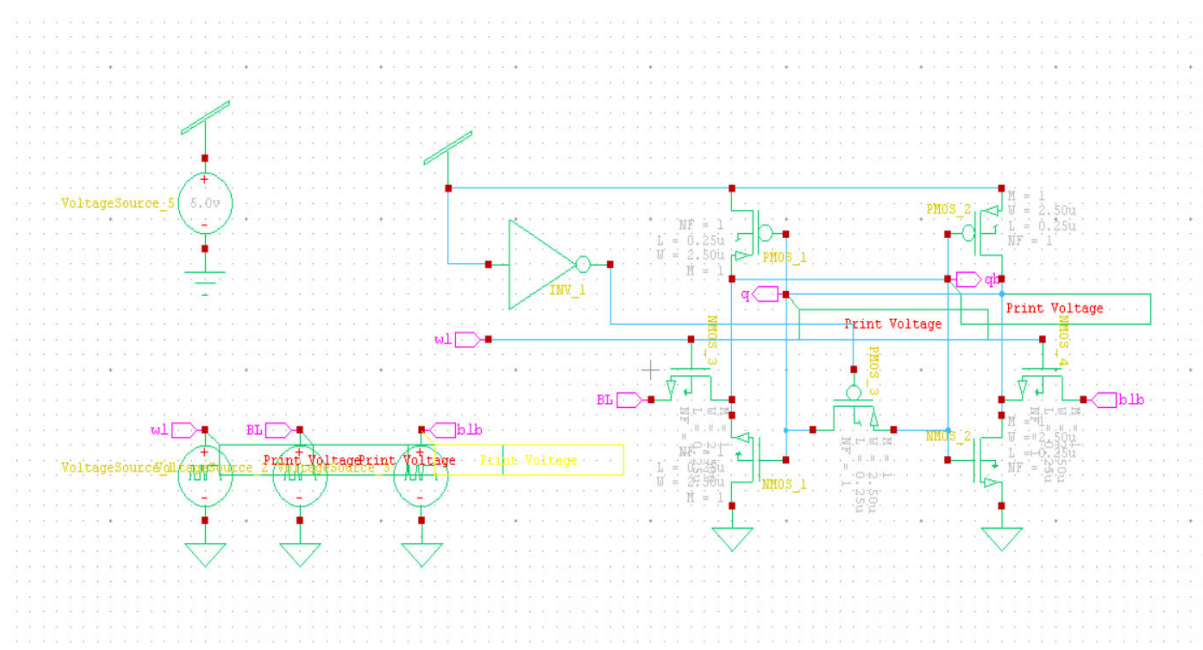


Figure 6. Schematic Model of 7T SRAM

Fig. 7 is a waveform example of a write operation that involves two phases. The top waveform depicts the writing of a '1' into a cell that was previously holding a '0'. In typical 6T SRAM cells, the internal Q and QB voltages are displayed



for comparison. Before applying power to the cells in a single word, the PC voltage is first asserted. The increased voltage reduces  $V_{DD}$ , which causes equalization of the internal Q-7T and QB-7T voltages via charge sharing. This last stage restores  $V_{DD}$  and activates the WL to allow writes to the cell. Set to  $V_{DD}$  and GND, respectively, the BL and BLB (already in that configuration) are then moved to Q-7T and QB-7T, where they are used to finish the write process. The voltage of the internal cells of a 6T cell, Q-6T and QB-6T, is only altered when the  $W_L$  is asserted, which means the energy of writing '1' and '0' operations is drastically different. The svc

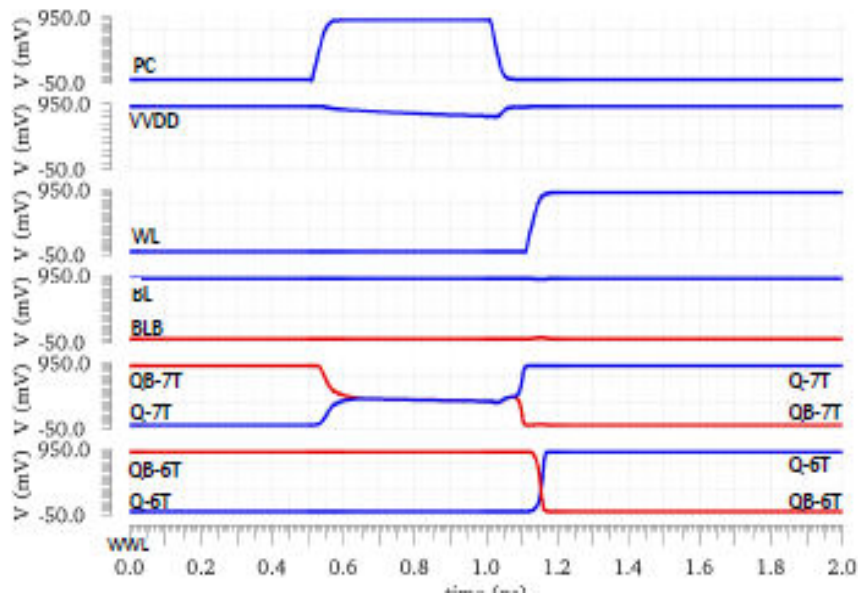


Figure 6. Waveform illustration of the 7T SRAM write operation

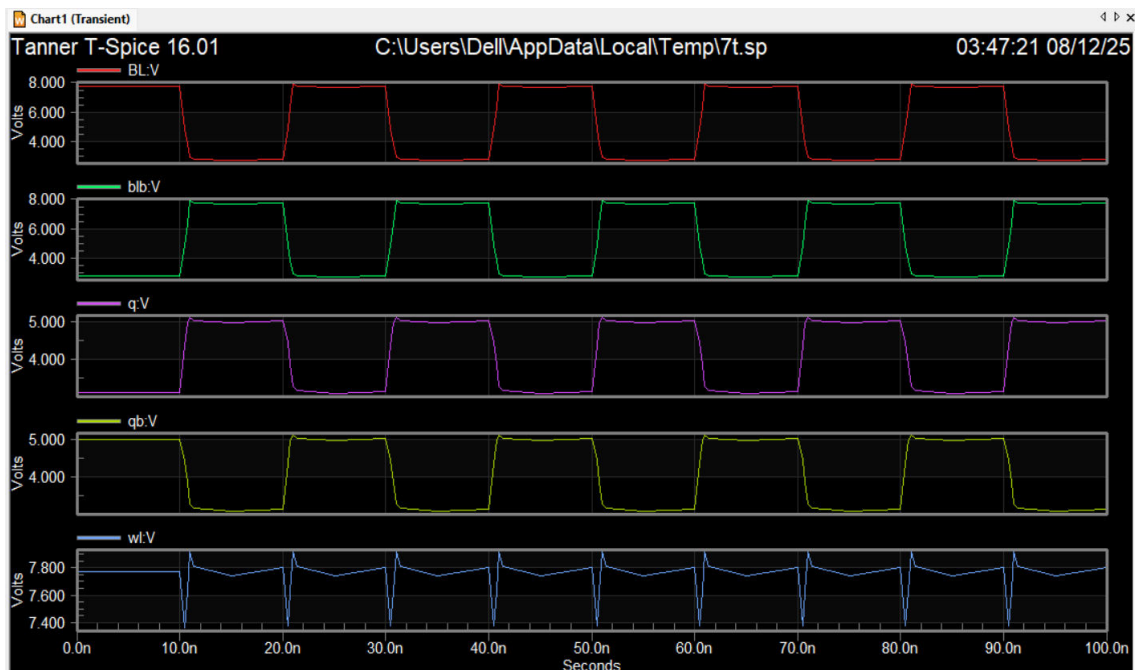


Figure 7. Waveforms of the proposed differential 7T SRAM including a replica BL



The area utilized for design of 7T SRAM is shown in table 1.

Table 1. Area utilization for 7T SRAM

Device	count
MOSFETs	9
MOSFET geometries	3
Voltage sources	4
Subcircuits	1
Model definitions	2
Computed models	2
Independent nodes	4
Boundary nodes	5

#### Adiabatic 7T SRAM:

The schematic diagram of adiabatic 7T SRAM is shown in figure 8.

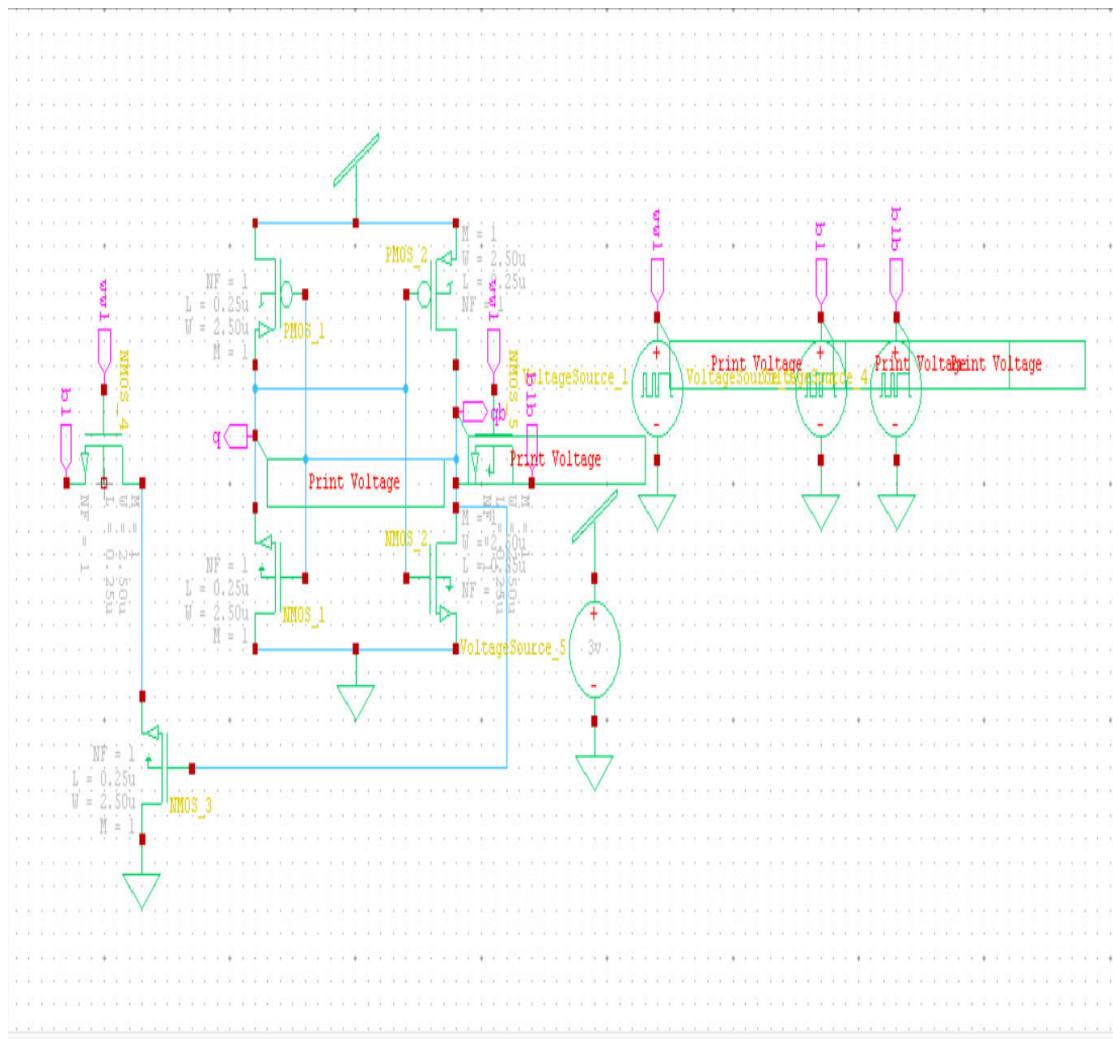


Figure 8. Schematic diagram of Adiabatic 7T SRAM

The waveform of the designed adiabatic 7T SRAM is shown in figure 9.

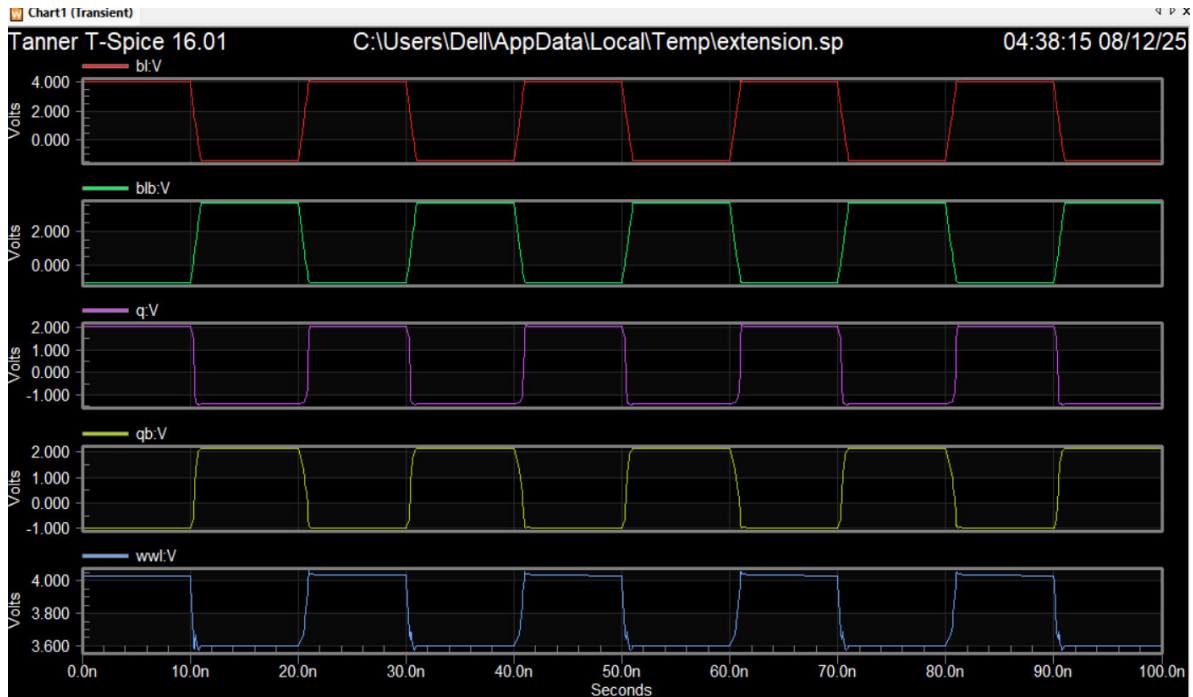


Figure 9. Waveforms of the Adiabatic 7T SRAM including a replica BL and polarity inter change

The area utilized for design of Adiabatic 7T SRAM is shown in table 2.

Table 2. Area utilization for Adiabatic 7T SRAM

Device	count
MOSFETs	7
MOSFET geometries	2
Voltage sources	4
Subcircuits	0
Model definitions	2
Computed models	2
Independent nodes	5
Boundary nodes	5

### Power Analysis

Because the 7T cell has an equalizing, symmetric structure, equalization phase current use is independent of any data previously stored in the cell. The power used prior to the WL assertion is the same whether or whether '1' or '0' had already been stored in the cell. With regards to the write '1' and '0' operations illustrated in Fig. 10(a), nearly similar waveforms are seen because of the two-phase write operation, showing that the information leakage from the currents dissipated in the 7T SRAM cell is non-existent. Fig. 10(b) shows the 1000 Monte Carlo simulations used to produce the write energy scatter plot of the 7T SRAM cell, which was derived using imperfect device matching and process variations. These estimates vary greatly from values obtained for the 6T SRAM cell, which show that the mean energy dissipations for the write '0' and '1' operations are 2.297 fJ and 2.301 fJ with a standard deviation of 0.0345 fJ and 0.353 fJ.

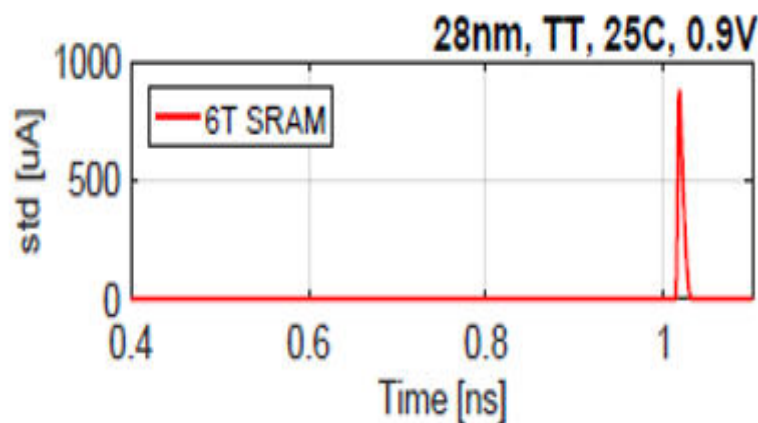
The total energy of an m-bit phrase stored in a memory row may be determined by determining the write energy dissipation and the amount of data stored. The total energy dissipation in m-bit words that are stored in an array is proportional to the Hamming value of the stored data, which is given by,

$$E_{w_{word}} = H_w \cdot E_C + (m - H_w) \cdot E_{NC} \quad (1)$$

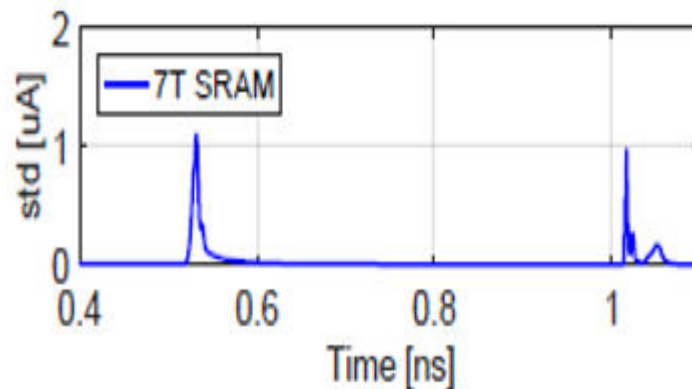
When m is the word longitude,  $E_C$  and  $E_{NC}$  are written energy dissipations where the data stored inside the cell is altered or unchanged and  $H_w$  is the hamming weight of a word equivalent to the hamming distance provided between the word value and BL voltages.

$$H_w = HD(BL, Q) = \sum_i (BL_i \neq Q_i) \quad (2)$$

Writing simulations of 32 distinct  $H_w$  values were performed to 7T and 6T SRAM cells to assess the safety of the 32-bit memory word, and standard deviations between current traces were calculated. The amount of the data leakage is typically estimated by this methodology. The standard deviation curves produced are shown in Fig. 6. The percent overshoot for the 7T SRAM cell was 1.1  $\mu A$ , nearly three magnitude orders lower than for the 6T SRAM cell at 875  $\mu A$ . For power cut and feedback cut Bit cells, comparable maximum deviations were observed in comparison to the 7T cell at 2.1  $\mu A$  and 0.99  $\mu A$  respectively.



(a)



(b)

Figure 10. Standard Deviation of the current consumption of the SRAM Cell (a) 6T SRAM (b) 7T SRAM Cell

The power and delay results achieved for design of 7T SRAM is shown table 3.

Table 3. Power and delay in design of 7T SRAM

Parameters	Value
Average Power consumed	1.315755 e-014 wats
Max power	1.617323e-004
Mini Power	1.273821e-009
Delay in parsing	0.05 sec
Delay in setup	0.01 sec
Delay in DC operating point	0.09 sec
Transient Analysis	0.01 sec
Overhead	0.92 sec
Total delay	1.08 sec

The power and delay results achieved for design of Adiabatic 7T SRAM is shown table 4.

Table 4. Power and delay in design of Adiabatic 7T SRAM

Parameters	Value
Average Power consumed	6.851908e-013 wats
Max power	3.770196e-003
Mini Power	1.655326e-008
Delay in parsing	0.05 sec
Delay in setup	0.02 sec
Delay in DC operating point	0.07 sec
Transient Analysis	0.01 sec
Overhead	0.82 sec
Total delay	0.97 sec

#### IV. CONCLUSION

Incorporated memories with 6T SRAM screens occupy a significant part of cryptographic systems, which may store secret data; specific design measures are necessary to provide resilience against PA assaults. In this article we presented a new SRAM 7T cell consisting of an extra PMOS transistor that was integrated in the original 6T SRAM execution and a sequence operation to substantially decrease the connection between the energy used and the written data. The suggested 7T Ram cell achieves an energy correlation of more than 1000 lower than traditional 6T SRAM. In addition, the suggested 7T SRAM achieves 39 percent–53 percent reduced energy dissipation using a voltage leveling mechanism during pre-charges during written operation and 19 percent–38 percent less write time than existing PA-resistant SRAM bit.

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